What is claimed :

1. A flash memory system comprising:

an array of flash memory cells;

a first local bit line coupled to a first column of flash memory cells;

a second local bit line coupled to a second column of flash memory cells;

a third local bit line coupled to a third column of flash memory cells;

a fourth local bit line coupled to a fourth column of flash memory cells, wherein the first, second, third and fourth local bit lines are positioned generally parallel with each other;

a first global bit line;

a second global bit line;

first, second, third and fourth select transistors, the first select transistor is coupled to the first local bit line and the first global bit line, the second select transistor is coupled to the second local bit line and the second global bit line, the third select transistor is coupled to the third local bit line and the first global bit line, the fourth select transistor is coupled to the fourth local bit line and the second global bit line;

a first select line to activate the first and second select transistors; and

a second select line to activate the third and fourth select transistors.

2. The flash memory system of claim 1 wherein the first and third select transistors are located at opposite ends of the array from the second and fourth select transistors.

3. The flash memory system of claim 1 wherein the local bit lines are formed on a first metal level and the global bit lines are formed on a second metal level.

4. The flash memory system of claim 1 wherein the array of flash memory cells is positioned adjacent the multiplex circuit.

5. The flash memory system of claim 1 wherein each of the flash memory cells is comprised of a floating gate capable of holding a charge.

6. The flash memory system of claim 5 wherein a presence or absence of the charge determines a state of the flash memory cell.

7. A flash memory system comprising:

an array of flash memory cells;

a first local bit line coupled to an associated first column of flash memory cells;

a second local bit line coupled to an associated second column of flash memory cells;

a third local bit line coupled to an associated third column of flash memory cells;

a fourth local bit line coupled to an associated fourth column of flash memory cells, wherein the first, second, third and fourth local bit lines are positioned generally parallel with each other;

a first global bit line;

a second global bit line;

first, second, third and fourth select transistors, the first select transistor is coupled to the first local bit line and the first global bit line, the second select transistor is coupled to the second local bit line and the second global bit line, the third select transistor is coupled to the third local bit line and the first global bit line, the fourth select transistor is coupled to the fourth local bit line and the second global bit line;

a first select line to activate the first and second select transistors; and

a second select line to activate the third and fourth select transistors.

8. The flash memory system of claim 7 and further including twice as many local bit lines as global bit lines.

9. The flash memory system of claim 8 wherein each global bit line is selectively coupled to alternating local bit lines.

10. The flash memory system of claim 7 wherein each of the local bit lines are formed on a first metal level and each of the global bit lines are formed on a second metal level.

11. The flash memory system of claim 7 wherein the system is manufactured such that each of the local bit lines are on a different level than the global bit lines.

12. The flash memory system of claim 7 wherein the first, second, third, and fourth select transistors comprise a first multiplex circuit.

13. The flash memory system of claim 7 wherein the select lines are coupled to a control gate of each of the first, second, third, and fourth select transistors.

14. The flash memory system of claim 12 wherein the array of floating gate memory cells is located between the first multiplex circuit and a second multiplex circuit.

15. The flash memory system of claim 7 wherein the first, second, third, and fourth select transistors are located at opposite ends of the array of flash memory cells.

16. The flash memory system of claim 7 wherein at least one local bit line of the first, second, third, and fourth local bit lines is located above a drain diffusion region.

17. The flash memory system of claim 13 wherein the array of floating gate memory cells is arranged in rows and columns.